Docket No.: GR 98 P 1513

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MAIL STOP: APPEAL ~~BRIEF-PATENTS~~

By: _____ Date: November 4, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

Applicant : Holger Hübner et al.

Applic. No. : 09/685,362

Filed : October 10, 2000

Title : Semiconductor Component Having a Material Reinforced Contact Area

Examiner : Matthew E. Warren - Art Unit: 2815

BRIEF ON APPEAL

Hon. Commissioner for Patents,
Alexandria, VA 22313-1450

S i r :

This is an appeal from the final rejection in the Office action dated June 2, 2003, finally rejecting claims 1-4 and 6-9.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $330.00 to cover the fee for filing the *Brief on Appeal*.

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-4 and 6-9 are rejected and are under appeal. Claim 5 was cancelled in an amendment filed on March 17, 2003.

Status of Amendments:

No claims were amended after the final Office action. *A Notice of Appeal* was filed on September 4, 2003 in response to the final Office action dated June 2, 2003.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention lies in the field of semiconductor technology and relates to a semiconductor component having first and second metal areas, which are both produced from a common first metal layer and

are electrically insulated from one another. A second metal layer which is produced separately from the first metal layer and has a third metal area which is insulated from the first metal layer by the interposition of a dielectric layer is provided, where, together with the dielectric layer and the first metal area, it forms a memory element. A fourth metal area is provided in the second metal layer which, together with the second metal area, forms a contact area, and is used to make contact with the second metal layer. The invention also relates to a method for manufacturing the semiconductor component.

Appellants explained on page 12 of the specification to Fig. 1 shows a semiconductor component 5 with a memory cell 10. The memory cell 10 is disposed on an intermediate oxide 15 and is formed in layers from a first metal area 20, a dielectric layer 25 and a third metal area 30, with the two metal areas 20 and 30 representing the electrodes of the memory cell 10. The first metal area 20 is seated on a barrier layer 35 in order to prevent oxygen diffusion into the dielectric layer 25. A contact area 40 is disposed at the side adjacent to the memory cell 10, and is formed from a second metal area 45 and a fourth metal area 50, which makes direct contact with it. The third metal area 30 and the

fourth metal area 50 are electrically connected to one another.

As outlined on page 13 of the specification, line 4, the memory cell 10 and the contact area 40 are essentially formed from two successively deposited metal layers, by selective etching. For this purpose, the barrier layer 35 is deposited first of all onto a surface of the semiconductor component 5, followed by a first metal layer 20, 45. Once these two layers have been jointly structured, during which process the first metal area 20 and the second metal area 45 are formed, this is followed by the dielectric layer 25 being deposited over the entire area by a metal-organic chemical vapor deposition process (MOCVD).

Appellants also stated on page 13 of the specification, line 15, that, in a further method step, the dielectric layer 25, which is composed of a ceramic material having a high dielectric constant, is removed from the second metal area 45. A second metal layer 30, 50 is then deposited and is structured, with the fourth metal area 50 of the second metal layer covering the second metal area 45 where, together with the latter, it forms the contact area 40. The material thickness of the contact area 40 thus corresponds approximately to twice the material thickness of one of the

two metal layers. If the contact area 40 is formed in steps or depressions on the surface of the semiconductor component 5, the material thickness may advantageously be even greater, as well.

Appellants outlined on page 14 of the specification, line 2, that, in a subsequent method step, an intermediate oxide 60 is applied over the entire surface and is masked, after which contact holes are formed. A first contact hole 65 passes through the intermediate oxide 60 as far as the contact area 40, and two further contact holes 70 and 75, which are considerably deeper, additionally pass through the intermediate oxide 15. Since the contact area 40 has twice a material thickness, the etching process in the area of the contact hole 65 is delayed to a sufficient extent during the formation of the contact holes 65, 70 and 75 to prevent the over etching which is required there leading to the contact area 40 being etched through. The contact holes 65, 70 and 75, which are of different depths, can thus be produced in a joint etching process without using an additional resist layer on the contact area 40.

Appellants further outlined on page 14 of the specification, line 18, that the opening 65 can be filled with an

electrically conductive material 100 for making contact with the contact area 40.

It is stated in the last paragraph on page 14 of the specification, line 21, that Fig. 2 shows the semiconductor component 5 in which the contact area 40 is formed by the interposition of the dielectric layer 25. Here, in order to simplify the process further, the dielectric layer 25 and the second metal layer have been structured together. The second metal area 45, the dielectric layer 25 and the fourth metal area 50 now act jointly as an etching resist. This layer structure of the contact area 40 also prevents complete etching through, to a sufficient extent. If the fourth metal area 50, which is located above, is completely or partially etched through, which may occur, contact is made with it in the contact hole 65 on an annular rim 90 formed by it. The area of the rim 90 presented to the contact hole is in the same order of magnitude as its cross section, particularly in the case of contact holes having a small cross section.

Appellants described on page 15 of the specification, line 11, that platinum alloys or platinum are preferably used for the two metal layers. In consequence, ferroelectric materials, such as strontium bismuth tantalite, can also be

used for the dielectric layer 25, and these contribute to an improved specific storage density.

As stated in the last paragraph on page 15 of the specification, line 17, that the contact area 40 can be used to make contact with one or more of the memory cells 10. The electrically conductive connection between the contact area 40 and the memory cells 10 is produced by conductor tracks 80 which are formed during the structuring of the second metal layer 30, 50. In consequence, the contact area 40 and the memory cells 10 may also be physically separated well away from one another. On the other hand, an electrically conductive connection may also be left between the first metal area and the contact area 40, in which case the conductor tracks 80 are then produced from the first metal layer.

Appellants explained in the last paragraph on page 16 of the specification, line 4, that, in principle, the contact areas according to the invention can also be used to make contact with other components on the semiconductor component 5. For this purpose, the metal areas 45 and 50 which are electrically insulated from the memory cell 10 remain on the surface of the semiconductor component 5 after the etching of the first and second metal layer, and are used as wiring to

make contact with further components, with the material in the contact areas of this wiring being reinforced by the first and the second metal layers being located one on top of the other.

References Cited:

U.S. Patent No. 5,563,762 (Leung et al.), dated October 8, 1996;

U.S. Patent No. 5,972,788 (Ryan et al.), dated October 26, 1999.

Issues

1. Whether or not the references Ryan et al. (U.S Patent No. 5,972,788) (hereinafter "Ryan") and Leung et al. (U.S. Patent No. 5,563,762) (hereinafter "Leung") can be properly combined under 35 U.S.C. §103.

2. Whether or not claims 1-4 and 6-9 are obvious over Ryan (U.S Patent No. 5,972,788) in view of Leung (U.S. Patent No. 5,563,762) under 35 U.S.C. §103.

Grouping of Claims:

Claim 1 is independent. Claims 2-4 and 6-9 depend on claim 1. The patentability of claims 2-4 and 6-9 is not separately argued. Therefore, claims 2-4 and 6-9 stand or fall with claim 1.

Arguments regarding the combination of Ryan and Leung:

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, *inter alia*:

the second metal layer having an electrically conductive connection between the third metal area and the fourth metal area.

The Ryan reference discloses an electronic device including an interconnect and a capacitor, both including respective portions of a first metal layer, a dielectric layer and a second metal layer, and further including a connection to both the first metal layer and the second metal layer of the interconnect and a connection to each of the first metal layer and the second metal layer of the capacitor (column 3, lines 55-62).

The object of Ryan is to form a metal-to-metal **precision capacitor** and interconnects resistant to metal migration in the same process (column 3, lines 39-42). A precision

capacitor is a capacitor for analog circuits (column 3, lines 6-17). Furthermore, Ryan discloses that "While such a variation in capacitance and voltage limitation is generally tolerable in digital circuits, there are many types of analog circuits in which variation in capacitance with voltage is not tolerable and requires metal plates to increase carrier concentrations" (column 3, lines 12-17).

Therefore, a person of ordinary skill in the art would consider the capacitor of Ryan as being a capacitor for analog devices. This point of view is further supported by the statement that "such a capacitor plate is generally **at least several times** the width of a conductor" (column 6, lines 7-10).

Contrary thereto, a capacitor forming a memory element is typically very small, since memory elements are tightly packed to obtain a high memory density.

Furthermore, the word "memory" is only used in conjunction with information storage, as the enclosed pages of The Random House Dictionary and Semiconductor Memories indicate.

Based on the above-given comments, appellants do not consider the capacitor of Ryan to be a memory element. Therefore, a

person of ordinary skill in the art would not combine the teachings of Ryan and Leung.

Arguments regarding the patentability of claim 1:

The combination of Ryan and Leung does not lead to the invention of the instant application as recited in claim 1 of the instant application for the following reasons.

Ryan discloses the formation of interconnects comprising two metal layers, which are insulated from each other by a dielectric layer. This dielectric layer is the key in overcoming the problems associated with electromigration and metal migration (column 6, lines 39-46). Therefore, a person of ordinary skill in the art would be taught to integrate a dielectric layer between two metal layers.

Contrary thereto, Leung allows a direct connection between the metal areas (126) and the metal layer (134), which contradicts the teaching of Ryan.

Furthermore, a person of skill in the art would have had to remove the mandatory dielectric layer of Ryan in order to allow an electrical connection of the upper metal layer (134) from underneath.

Finally, Leung teaches placing a (analog) capacitor (as a filter element) "on top of the passivation layer of an otherwise completed integrated circuit" (column 3, lines 45-48). Therefore, an interconnect simultaneously formed with a capacitor as disclosed in Ryan is explicitly excluded by the teaching of Leung.

Regarding the second metal layer having an electrically conductive connection between the third metal area and the fourth metal area, as recited in claim 1, it is noted that Ryan simultaneously forms an interconnect and a capacitor. There is no electrical connection by either of the two metal layers M1 and M2 between either of the electrodes of the capacitor and the interconnect. Furthermore, Ryan provides no motivation for such a direct connection.

Another aspect refers to the kind of electrical connection of the upper and lower electrode. The upper and lower electrodes (21 and 22) of Ryan are directly contacted by metal studs (14 and 32), respectively. According to the arguments provided by the Examiner, a person of ordinary skill in the art would leave an electrical connection between the upper electrode (22) and the upper layer (25) of the interconnect (23) of Ryan to provide a contact area to

contact the upper electrode (22) in view of Leung. Appellants disagree with this assertion for the following reasons.

Leung provides an on-chip capacitor. Therefore, a simultaneous formation of an interconnect contradicts the teaching of Leung. A person of ordinary skill in the art would not combine the teachings of Ryan with those of Leung.

On the other hand, if a person of ordinary skill in the art would place the capacitor on top of a chip, no insulating layer covering the contact area and the memory element and having at least one opening formed therein and leading to said contact area, as recited in claim 1 of the instant application would be present.

Finally, Ryan already discloses how to connect the upper electrode. This is accomplished by a direct connection with a metal stud formed within an inter-level dielectric (31). However, Ryan does not provide any motivation, which would lead a person of ordinary skill in the art to provide a metal area outside the upper electrode, which can be used to contact the upper electrode. An electrical connection between the upper electrode (22) and the upper metal layer

(25) of the interconnect (23), which might be used as such a contact area is far beyond the scope of Ryan.

Since claim 1 is believed to be allowable, dependent claims 2-4 and 6-9 are believed to be allowable as well.

Based on the above-given arguments the honorable Board is respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

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For Appellants

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Appendix - Appealed Claims:

1. A semiconductor component, comprising:

a first metal layer forming a first metal area and a second metal area electrically insulated from one another;

a dielectric layer;

a second metal layer produced separately from said first metal layer and forming a third metal area insulated from said first metal layer by an interposition of said dielectric layer, and said third metal area together with said dielectric layer and said first metal area forms a memory element, said second metal layer further forming a fourth metal area which together with said second metal area forms a contact area used to make contact with said second metal layer and said second metal layer having an electrically conductive connection between said third metal area and said fourth metal area;

an insulation layer covering said contact area and said memory element and having at least one opening formed therein and leading to said contact area; and

an electrically conductive material filling said opening for making contact with said second metal layer.

2. The semiconductor component according to claim 1, wherein said contact area is used as an etching resist during etching of said opening.

3. The semiconductor component according to claim 1, wherein said fourth metal area makes direct contact with said second metal area.

4. The semiconductor component according to claim 1, wherein said fourth metal area is insulated from said second metal area by the interposition of said dielectric layer.

6. The semiconductor component according to claim 1, wherein said first metal layer and said second metal layer are composed of a noble metal.

7. The semiconductor component according to claim 1, wherein said dielectric layer is composed of a material selected from the group consisting of a ceramic material having a high dielectric constant and a ferroelectric ceramic material.

8. The semiconductor component according to claim 1, wherein at least one further opening is formed in said insulation layer.

9. The semiconductor component according to claim 6, wherein said noble metal is selected from the group consisting of platinum and platinum alloys.